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Loss Modeling of GaN Transistors Using Datasheet Data

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Original scientific research article

Highlights

- Development of a loss-estimation algorithm for GaN power transistors
- Comparison of hard, soft, and semi-soft switching processes, with separation of channel current and parasitic capacitance contributions
- Validation of the model through a 1 kW synchronous buck converter prototype

Abstract

Transistors based on modern wide-bandgap semiconductors, such as Gallium Nitride (GaN), are increasingly used in power electronics devices. Due to their specific structure and ability to rapidly switch states, standard calculations used for determining losses in silicon transistors are not applicable in this case. Therefore, an analytical model has been developed to estimate losses in GaN transistors in a half-bridge configuration, relying on data from technical documentation. The model considers different types of switching, including hard, soft, and semi-soft switching. A comparison of losses during soft and hard switching of transistors in a synchronous buck converter under the same operating conditions has been conducted. Finally, the proposed model has been verified through the design of a 1 kW buck converter.

Keywords

GaN transistors, loss model, synchronous buck converter

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1. INTRODUCTION

Decades of progress in development of power electronics devices have resulted in almost full exploitation of the potential of power transistors based on silicon (Si) technology. Therefore, further development of converters that rely on this type of semiconductors has become much more complex. However, development of transistors using wide band gap semiconductors, such as gallium nitride (GaN) and silicon carbide (SiC), has paved the way for the design of new topologies, as well as reaching higher efficiency and smaller converter dimensions [1]. As shown in Figure 1, GaN semiconductors, compared to Si and SiC, are characterized by higher electronic mobility, higher maximum electron velocity, and a larger breakdown field, [1].

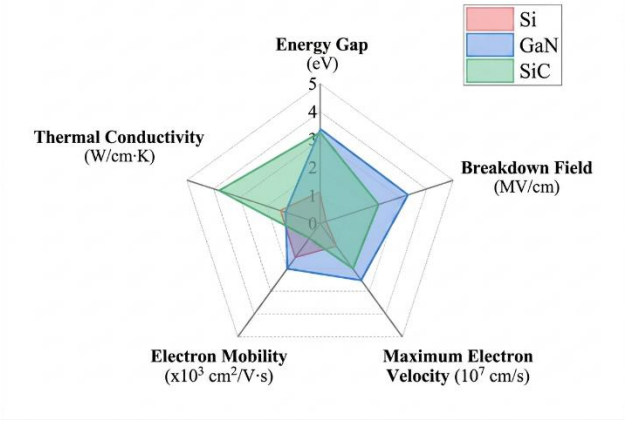


Figure 1. A comparative analysis of semiconductors technology, [1]

Considering that the GaN material has a significantly wider band gap and breakdown field compared to silicon semiconductors, it is possible to design a shorter conducting channel within a transistor for the same breakdown voltage value. A shorter conduction channel, coupled with a higher packing density of GaN transistor, results in lower conducting channel resistance and reduced parasitic capacitances. These properties provide lower power losses during switching on and off processes, which enables significantly higher switching frequencies to be achieved, [2].

To exploit the full potential of GaN transistors, it is necessary to create a reliable physical model that describes the switching process, in order to determine the total power losses and the maximum switching frequency. The switching models developed so far for Si transistors are not applicable to GaN devices, since the chemical and physical structure of these transistors is different, [2], [3]. The switching processes of GaN and Si transistors, although similar at first glance, differ considerably. Gallium nitride technology allows for a higher switching rate, whereby the influence of nonlinear parasitic capacitances becomes significant and cannot be disregarded. In addition, the conduction principles and the establishment of the conduction channel differ compared to silicon transistors. In [4], a piecewise linear model of losses is shown. This approach provides quick and easy estimation of losses but does not take into account the nonlinear dependence of parasitic capacitances on the corresponding voltages, which leads to significant errors in the estimation of switching losses in the band of several hundred kilohertz. A more detailed model of losses is presented in [5] and takes into account the nonlinear dependence of parasitic capacitances but disregards the nonlinear transconductance dependence of GaN power transistors. Considering these limitations, in this paper, an analytical switching model of GaN transistors has been developed, which at the same time takes into account the nonlinear dependencies of parasitic capacitances and transconductances, and enables precise determination of the total power losses on the transistor compared to currently available solutions in literature. The developed model is based on non-approximate data from the manufacturer's technical documents and takes into account the physical structure of the transistor.

Chapter 2 describes the model of GaN transistor and the physical dependencies between the modeled elements. During modeling, for a more precise determination of losses, the total current of the transistor was grouped into two contributions – the current of the conductive channel and the current of parasitic capacitances. Namely, during switching, not all current flows only through the conduction channel of the power transistor. A significant portion of the current, especially in the transition phases, goes to charging and discharging of the parasitic capacitance of the device, which directly affects the dynamic behavior of the transistor and affects the overall switching losses. Therefore, this classification, in addition to taking into account the nonlinear capacitances and transconductance of GaN power transistors, is crucial for realistic modeling and accurate estimation of power losses during a transistor operation. Also, switching on and off of switches is divided into phases and is described in detail for transistors in a half-bridge configuration. For the selected transistor in Chapter 3, there is an extraction of relevant data from the datasheet and an algorithm for estimating losses is given. Finally, the experimental results, confirming the reliability of the model, are given in Chapter 4.

2. MODEL OF THE TRANSISTOR AND SWITCHING PROCESS

Power transistors based on GaN technology, although their structure resembles the Si MOSFET (*Metal Oxide Semiconductor Field Effect Transistor*) devices, have certain characteristics that significantly affect their switching behavior. This chapter describes in detail the electrical model of GaN transistors with an emphasis on key differences compared to classic silicon MOSFET transistors. For the purpose of analytical modeling and calculation of transistor power losses, theoretical and analytical switching processes are described in detail in case of switching the transistors on and off in a half-bridge configuration. As a result, a system of differential equations is obtained, with which it is possible to determine the time forms of channel current $I_{ch}(t)$ and channel voltage $v_{ds}(t)$ required to calculate losses during the process of switching the transistors on and off. The GaN transistor model is shown in Figure 2 and largely corresponds to the Si MOSFET transistor model.

The main difference is the absence of a built-in diode for conducting current in the opposite direction. Due to their symmetrical structure, when conducting current in the opposite direction, the drain and source electrodes change their role. The drain electrode potential is now lower than the gate potential, so now the voltage v_{gd} dictates the conductivity of the channel and allows the transistor to conduct current. Further in the paper, this conduction mechanism will be called the inverse conduction of GaN transistors.

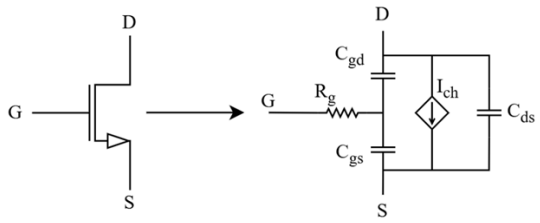


Figure 2. GaN transistor model

2.1 Switching process of power transistors in half-bridge configuration

Two transistors in a half-bridge configuration represent a universal switching cell in modern power converters, [1]. Although this configuration is not present in virtually every topology, most practical power converter architectures can be decomposed into cells in a half-bridge configuration or into some of their extended variants, [6]. In this subchapter, the switching process of two GaN transistors in a half-bridge configuration will be presented and explained in detail. Based on the derived model, an algorithm for estimating transistor power losses will be designed in Chapter 3.

Transistor switching in a half-bridge configuration is the process of changing current path from one transistor to another. To prevent a shoot-through between the upper and lower transistors in the half-bridge, the concept of dead time is introduced. This is the short time interval between the moment when one transistor is switched off and the moment the other transistor is switched on. Dead time ensures that the first transistor is completely switched off before a signal is sent to switch on the second transistor, effectively preventing the current conduction through both transistors at the same time. The switching process in the half-bridge configuration is conditioned by the operating mode of the inverter, that is, the direction of current through the transistor to be switched off. Two different types of switching can be distinguished, where the main difference between them is reflected in the direction of the current through the transistor channel I_L at the time of switching, as shown in Figure 3.

Switching type I is shown in Figure 3a and indicates that the current was present prior to switching, in the direction from the drain to the transistor source. Figure 3a shows an example of turning-off the upper switch in the half-bridge. After the conductive transistor is switched off, the current passes to the opposite transistor in the half-bridge. This type of switching off is known in literature as hard switching. Since the current cannot be switched instantaneously, in parallel with the described process, the opposite transistor marked with number 2 in Figure 3 takes over the current through its parasitic capacitance, since the direction of the current allows it. After the parasitic capacitance C_{ds} is completely discharged, transistor 2 conducts current by an inverse conduction mechanism, and this process continues until the rest of the dead time expires. When the dead time expires, this transistor can be switched on under zero-voltage conditions. This phenomenon is called soft switching, since the flow of the load current has naturally discharged the parasitic capacitance C_{ds}, [1]. We conclude that the switching type I is determined by the direction of the current from the drain to the transistor source and is characterized by a sequence of hard switching off – soft switching on.

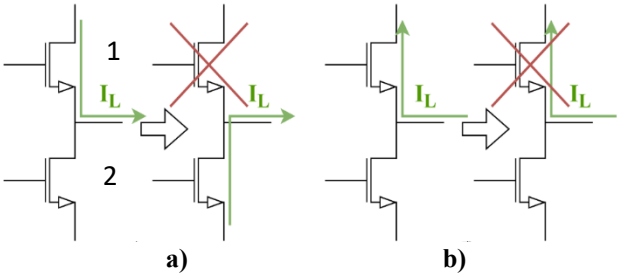


Figure 3. Types of switching for different current directions: a) "positive" current direction; b) "inverse" current direction

Switching type II (Figure 3b) indicates that the current through the semiconductor device has a direction from the source to the drain, whereby the current after the switching off continues to pass through the same transistor with the inverse conduction of the GaN transistor. This type of transistor switching off is known in literature as soft switching. Only the transition from a regular conduction mechanism to an inverse conduction mechanism is considered to be a lossless or soft process, but nevertheless conduction losses increase due to voltage increase v_{sd}. In this case, the capacitance C_{ds} of the second transistor is not discharged during dead time because there is no necessary current to make this possible, as in the first case. Switching on of the transistor that follows after the remaining dead time has elapsed is called hard switching on. We conclude that the switching type II is determined by the direction of the current from the source to the drain of the transistor and is characterized by a sequence of soft switching off – hard switching on.

Both types of switching process are given for the example of switching off the upper transistor – switching on the lower transistor in the half-bridge, but the same conclusions may be made for the opposite sequence without losing generality, by following the direction of the current through the conductive transistor.

For both cases, the GaN model shown in Figure 2 is considered. During the switching process, the transistor operates in ohmic mode. In this mode, the conduction channel can be modeled as a controlled current source I_{ch}, where the peak value of the current I_{ch} is related to the voltage v_{gs} via transconductance g_m. In all the described

switching processes, it is assumed that the output current of the half-bridge I_L does not change and remains constant for the duration of the switching process. The following sections will describe in detail both the switching on and switching off processes of the power transistor.

2.2 Transistor switching off

Switching off process of the GaN transistor is described separately for switching types I and II. Each of these switching off processes is separated into specific stages to provide an accurate analysis of transistor behavior and transient losses. In this way, it is possible to understand the dynamics of the device and later optimize the control signals to achieve maximum efficiency.

2.2.1 Switching type I – hard switching off

As explained in Section 2.1, transistor switching off during the switching type I means that the switching current I_L is taken by the second transistor in the half-bridge. This case is divided into three phases as shown in Figure 4. This type of switching occurs when the current I_L is positive, that is, it has a direction from the drain to the source of the conductive transistor.

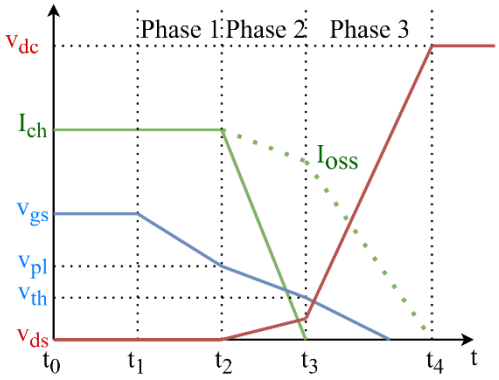


Figure 4. Switching type I – hard switching off

During phase I, the driver received a switching off command and began to reduce the voltage v_{gs}. Voltage v_{gs} changes its value according to the following law:

$$v_{gs} = v_{dr\_on} \cdot e^{-\frac{t}{R_e C_{gs}}}, \qquad (1)$$

where v_{dr_on} is the switching on voltage of the transistor provided by the driver, and R_e the total resistance of the gate loop circuit and is the sum of the self-resistance of the transistor gate, the external resistor of the driver circuit, and the driver output resistance.

During this phase, a constant current $I_{ch} = I_L$ passes through the conduction channel of the transistor. The transistor is saturated all the time during phase I, so the current of the channel does not depend on the voltage v_{gs}. At the time when the voltage v_{gs} is equal to the Miller plateau voltage v_{pl}, where the v_{pl} voltage corresponds to the current I_L at the transfer characteristic of the transistor shown in Figure 5, phase I ends. At that time, the transistor exits the saturated operating mode and begins to operate in the ohmic region where the channel current I_{ch} is directly proportional to the gate voltage, v_{gs}.

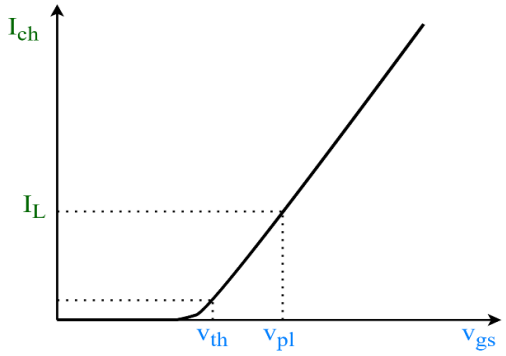


Figure 5. Current-voltage characteristic of GaN transistor

During phase II, the voltage v_{gs} continues to drop but its drop is slowed down because the driver at this point begins to charge the parasitic capacitance, as shown in Figure 6.

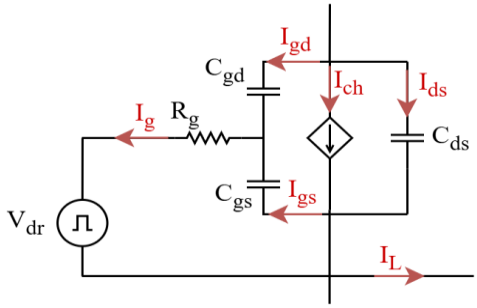


Figure 6. Current directions in GaN transistor model during phase II

The differential equation describing the change v_{gs} is given by (2), [7]:

$$\frac{dv_{gs}}{dt} = \frac{I_g}{C_{gd}+C_{gs}} - \frac{C_{gd}}{C_{gd}+C_{ds}} \cdot \frac{(I_L - I_{ch})}{2} \cdot \frac{1}{(C_{gd}+C_{gs})}, \qquad (2)$$

while the current of the channel I_{ch} changes non-linearly with the change of v_{gs}, according to the transfer characteristic shown in Figure 5. It is important to note that all parasitic capacitances of transistors, such as C_{gs}, C_{gd} and C_{ds}, are not constant, but represent nonlinear functions of the corresponding voltages. Therefore, for an accurate analysis at any time, it is necessary to know the actual values of voltages v_{gs}, v_{ds} and v_{gd} to accurately determine the values of these capacitances. Since the value of v_{gs} is known at any time, it is necessary to determine both v_{ds} and v_{gd}. The voltage $v_{ds}(t)$ can be determined by solving the following differential equation, [1]:

$$\frac{dv_{ds}}{dt} = \frac{I_L - I_{ch}}{C_{oss1}+C_{oss2}}, \qquad (3)$$

where both C_{oss1} and C_{oss2} are the output capacitances of the transistor and represent the sum of C_{ds} and C_{gd}. Voltage v_{gd} is obtained as the difference of the voltage v_{gs} and v_{ds}.

Phase II lasts until the channel current I_{ch} drops to zero, more precisely until the voltage v_{gs} reaches the conduction threshold voltage v_{th}.

During phase III, the conduction channel of the transistor is closed, but the total current through the transistor is non-zero until the parasitic capacitances C_{ds} and C_{gd} are loaded. The equations given for phase II are still valid for phase III with the fact that now $I_{ch} = 0$.

2.2.2 Switching type II – soft switching off

During the switching type II (Figure 3b), the active transistor switches off, but all current continues to flow through it due to the process of inverse conduction of the GaN transistor. This process represents the transition of the transistor from saturated mode to inverse conduction mode, is shown in Figure 7 and is divided into two phases.

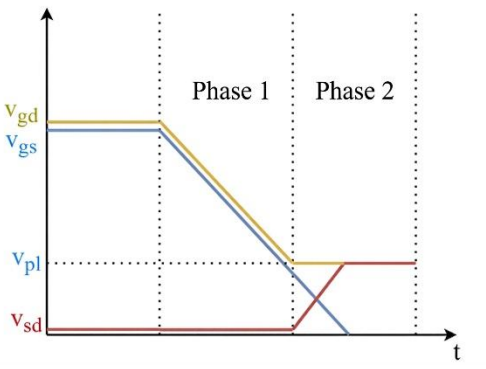


Figure 7. Switching type II – soft switching off

This type of switching can occur only if the current I_L is negative, that is, if the current direction is from the source to the drain of the conductive transistor (Figure 3b). In this type of switching, the voltage v_{sd} does not rise to the voltage v_{dc} but to the voltage of the inverse conduction of the GaN transistor. For low-power devices, this voltage is several volts.

Phase I is identical to the first switching type, and its phase I described in Subchapter 2.2.1, so that the voltage v_{gs} varies according to the law described in equation (1). The voltage v_{gd} during this phase is equal to the sum of the voltage v_{gs} and v_{sd}. The voltage drop across the conduction channel v_{sd} during this phase is constant and is equal to the product of the resistance of the conduction channel R_{ds_on} and the channel current I_{ch}.

Phase II begins when the voltage v_{gd} reaches the Miller plateau v_{pl}, that is, the voltage corresponding to the current I_L at the transfer characteristic given in Figure 3. After that time, the voltage v_{gd} remains constant. The voltage v_{gs} continues to change according to equation (2). Since the voltage v_{gd} is constant and the voltage v_{gs} drops, the voltage drop across the conduction channel of the transistor v_{sd} during this phase will increase and can be determined by the following equation:

$$v_{sd} = v_{gd} + v_{sg} \,. \tag{4}$$

2.3 Transistor switching on

When switching on the power transistor, two types of switching are again distinguished – when the current I_L has a positive (from the drain to the source) and when it has an inverse (from the source to the drain) direction (Figure 2). Each of these processes, similar to switching analysis, is divided into phases. The division into phases provides a precise understanding of the dynamics of the device during the transition from the off to the on state, which will later be necessary for an accurate estimation of switching losses and performance optimization.

2.3.1 Switching type I – soft switching on

During the transistor switching on during the switching type I (Figure 3a), it is normal that its parasitic capacitances C_{ds} and C_{gd} are both discharged (during switching off the opposite switch) and that a current I_L passes through the transistor by inverse conduction. This case is divided into two phases as shown in Figure 8.

During phase I, the voltage v_{gd} is constant and corresponds to the voltage of the Miller plateau for current I_L, while the voltage v_{gs} rises according to the equation:

$$v_{gs} = v_{dr_{on}} \left(1 - e^{-\frac{t}{R_e C_{gs}}}\right). \tag{5}$$

At the time instant when the voltage v_{gs} reaches the Miller plateau voltage for current I_L, the inverse conduction of the GaN transistor stops and now the active area is fully conductive and allows current to pass in both directions. During phase II, the voltage continues to rise according to the dynamics shown in (5) and reaches the value of v_{dr_on}.

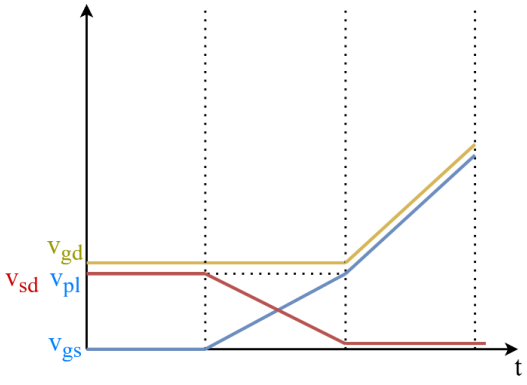


Figure 8. Switching type I – soft switching on

2.3.2 Switching type II – hard switching on

While transistor is switching on during the switching type II, Figure 3b, the parasitic capacitance C_{ds} and C_{gd} are not pre-discharged, as in the previous case, so they need to be discharged during the switching process. In this case, the switching on takes place in three phases, shown in Figure 9.

During phase I, the voltage v_{gs} rises to the voltage of the transistor conduction threshold v_{th}. During both phase

I and phase II, the voltage v_{gs} changes according to equation (5). When the current through the active area of the transistor begins to rise, phase II begins.

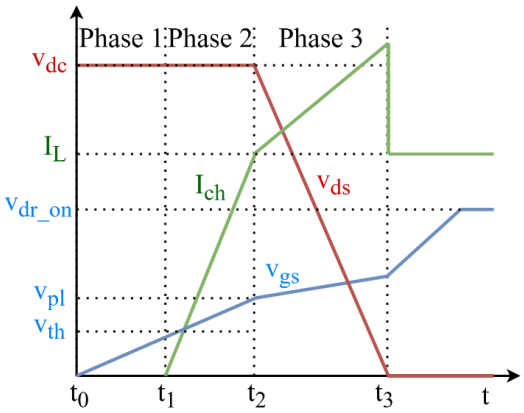


Figure 9. Switching type II – hard switching on

During phase II, the voltage v_{gs} rises from the conduction threshold voltage v_{th} to the Miller plateau voltage v_{pl} corresponding to the current I_L, while the current rises from zero to I_L. The relationship between voltage v_{gs} and current I_L is given in Figure 2. Until the transistor that switches on takes all the current from the transistor that is in the inverse conduction mechanism, there can be no change in voltage v_{ds}. The reason why this phenomenon develops is hidden in the inverse conduction mechanism itself, which does not allow the voltage drop in its active area to change as long as there is an inverse current flowing through the channel.

During phase III, the parasitic capacitances C_{ds} and C_{gd} are discharged by current through the active channel of the transistor, as shown in Figure 10.

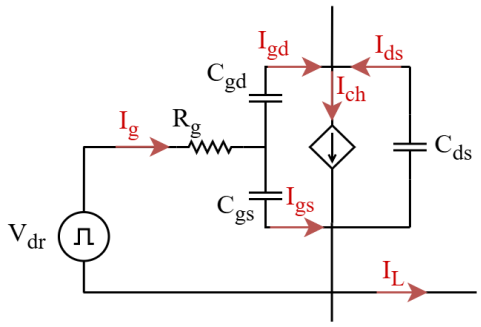


Figure 10. Current directions in the GaN transistor model during the switching type II process – switching on

During this phase, there is a significant increase in the current of the transistor active area $I_{ch,}$, so that the stress that the semiconductor suffers is significantly higher than the stress of the steady state operating mode. The current through the active region I_{ch} is related to the voltage v_{gs} via the graph given in Figure 10.

The rate of voltage v_{gs} change is now significantly slowed down because the current provided by the driver not only charges the capacitance C_{gs} but also discharges the capacitance C_{gd}. The change in voltage v_{gs} is given, [7] by:

$$\frac{dv_{gs}}{dt} = \frac{I_g}{C_{gd}+C_{gs}} - \frac{C_{gd}}{C_{gd}+C_{ds}} \cdot \frac{(I_{ch}-I_L)}{2} \cdot \frac{1}{(C_{gd}+C_{gs})}, \quad (6)$$

while the change in voltage v_{ds} is given by the equation:

$$\frac{dv_{ds}}{dt} = \frac{I_{ch}-I_L}{C_{oss1}+C_{oss2}}. \quad (7)$$

By solving the system of differential equations (1) - (7) and taking into account that the values of all parasitic capacitances are a function of their corresponding voltages, the time-domain waveforms of current $I_{ch}(t)$ and voltage $v_{ds}(t)$ are obtained. Current $I_{ch}(t)$ and voltage $v_{ds}(t)$ time waveforms are needed to accurately determine the losses at transistors.

3. LOSS CALCULATION

The key performance indicators of a power converter are efficiency, size, and price. Efficiency can be increased by selecting GaN semiconductor components with better static and dynamic characteristics than conventional Si transistors. Better dynamic characteristics provide operation at higher frequencies, which leads to a reduction in the required dimensions of passive components such as transformers, inductors, and capacitors. To take full advantage of GaN transistors, it is essential to develop a reliable model for calculating losses. Based on such a model, it is possible to determine which GaN transistor is most suitable for a specific application, whether additional cooling is required, which type of cooling is adequate, as well as the maximum operating switching frequency. In this chapter, a model for estimating losses based on previously derived equations and information collected from the transistor datasheet, will be developed.

Losses in transistors during a single switching cycle include losses in switching on, losses in switching off, losses in gate loop, losses during current conduction, and losses due to the reverse conduction mechanism. Figure 11 shows the waveforms of power losses during transistor hard switching on and switching off. It is important to note that the overlap of current and voltage is significantly more pronounced during transistor switching on, which is why the energy of losses during switching on is higher than when switching it off. In certain topologies, in which two switching transitions of the type I can be realized (Figure 3a), and which are characterized by a sequence of soft switching on and hard switching off within a single switching period, it is possible to greatly reduce the overall switching losses. In this case, during one period, two soft switching ons and two hard switching offs are obtained. This sequence is characteristic of LLC resonant converters, which can achieve very high efficiencies compared to other isolated DC/DC topologies by using GaN transistors. Although this mode of operation is common for LLC converters, it is also possible to implement it in a synchronous buck converter, under the conditions that will be discussed in detail in Chapter 3.2.

Total switching and conduction losses can be expressed as the product of the current flowing through the conduction channel of the transistor and the voltage drop across it:

$$P_{total} = \frac{1}{T_{PWM}} \int_0^{T_{PWM}} I_{ch}(t) \cdot v_{ds}(t) \cdot dt. \quad (8)$$

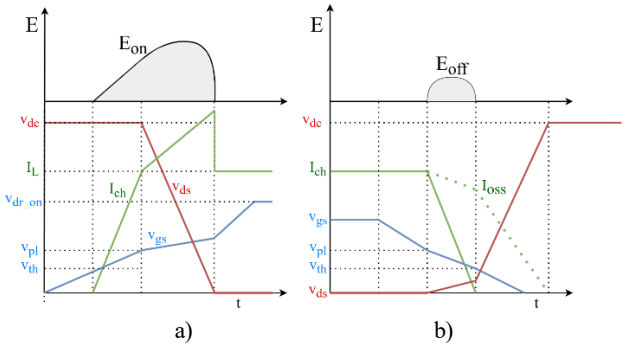


Figure 11. Losses energy during hard (a) switching on (b) switching off

In order to evaluate the power of the losses at the transistor, it is necessary to determine the time waveforms of quantities of importance in the function of operating modes. In order to determine the time waveforms of the channel current $I_{ch}(t)$ and the channel voltage drop $v_{ds}(t)$, it is necessary to solve the system of differential equations resulting from Chapter 2. In order for a system of equations (1) (7) to be solvable, it is necessary to know the following dependencies:

$I_{ch}(v_{gs})$ – dependence of the current of the transistor active area on the voltage v_{gs};

$I_{ch}(v_{gd})$ – dependence of the current of the transistor active area on the voltage v_{gd} during inverse conduction of current;

$C_{ds}(v_{ds})$ – dependence of the drain-source capacitance on the voltage drop in the transistor active area v_{ds};

$C_{gd}(v_{gd})$ – dependence of gate-drain capacitance on voltage v_{gd};

$C_{gs}(v_{gs})$ – dependence of gate–source capacitance on voltage v_{gs}.

The above dependencies can be precisely determined by experimental methods, such as the *double-pulse test*. However, this approach is often not practical because it involves purchasing a component and doing all measurements to verify its suitability for a particular application. Alternative ways include use of approximation expressions, the adjustment of curves, or, in the case of parasitic capacitances, the application of a charge-based model. Although experimental measurements are the most reliable source of data, they are the most difficult to obtain, while approximation methods often lead to significant discrepancies.

Therefore, a different approach is taken in this paper. Based on the curves given in the transistor datasheet, discrete values of the required quantities are determined using the *Automeris* software package. From these discrete dependencies and differential equations obtained by discretizing the expression (1) - (7), it is possible to determine the waveforms $I_{ch}(t)$ and $v_{ds}(t)$.

3.1 Acquisition of data from the datasheet

The data in the transistor datasheet is most often presented in the form of graphics, which are obtained based on measurements done by the manufacturer and then presented in the datasheet. If the manufacturer does not have tabular values of the required dependencies or is not willing to share them, it is necessary to extract the data directly from the graphics from the datasheet. In this paper, this procedure is done using a software package [8]. An example of how to use this tool is shown in Figure 12.

This software package is intended for the digitization of graphic data, i.e. the extraction of numerical values from graphic figures. This tool enables for the user to easily obtain tabular data suitable for further analysis and calculation from existing diagrams.

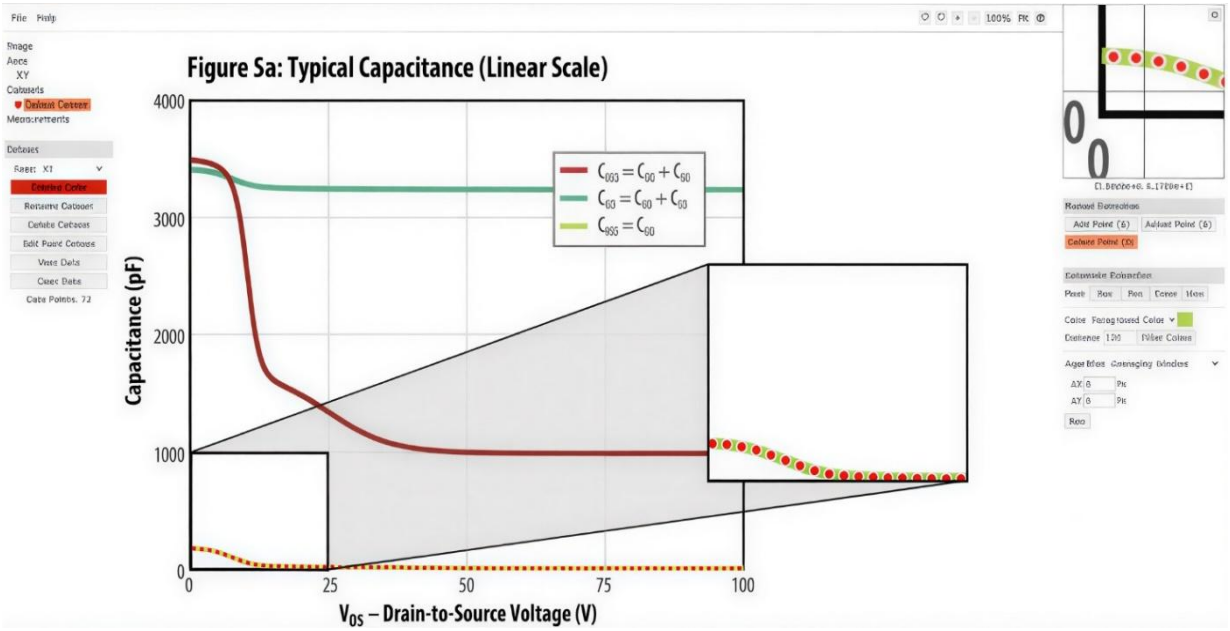


Figure 12. Using tools to extract data from the datasheet

The figure shows the change in parasitic capacitances extracted from the datasheet of a commercially available GaN transistor depending on the drain–source voltage v_{ds}. The software package was used to estimate discrete capacitance values at more than 100 points, which are marked with red dots, thus ensuring high accuracy of the dependencies shown.

3.2 Algorithm for estimating losses

Based on the differential equations derived in Chapter 2 and the data collected from the datasheet, it is possible to estimate the losses dissipated at the transistors. To determine the operating state of the transistor and the type of switching process that is currently being executed, it is necessary to know the current of the half-bridge I_L at any time. The current I_L does not depend directly on the type of transistor, but on the external parameters of the electrical circuit, such as the voltage of the DC link and the values of the passive elements and active load. By knowing the current I_L based on the algorithm shown in Figure 13, it is possible to determine the states through which the transistor passes during a single period of switching. The positive direction of the current means the current that has the direction from the drain to the source, while the negative direction of the current is from the source to the drain.

The result of the algorithm is the discrete values of the voltage drop on the conduction channel $v_{ds}(k)$ and the current of the conduction channel $I_{ch}(k)$, and the losses on that transistor over a switching period are determined based on the discretized equation (9).

$$P_{total} = \frac{1}{N}\sum_{k=0}^{N-1} I_{ch}(k) \cdot v_{ds}(k) \qquad (9)$$

3.3 Loss analysis

This chapter evaluates switching losses for the selected GaN transistor in the half-bridge configuration. The losses were determined and intercompared for two different values of current waves, in order to have an overview of the effect of different sequences of switching states on the overall power dissipation. For this purpose, scripts were developed in the software package [9], which enabled solving the system of differential equations obtained by discretizing expressions (1) – (7) using Euler's first-order discretization method. The states of the system were determined by applying the algorithm shown in Figure 13, which enabled study of the transistor losses in different operating modes of the converter.

The analysis of losses was made under the following conditions. The power of the converter is determined to be $P = 1$ kW, the input voltage is $V_{in} = 60$ V and the duty cycle $d = 0.75$, while other parameters of importance are given in Table I. The total losses on both transistors in the half-bridge configuration are given in Figure 14, for the case when the current ripple is higher than its mean value.

From the graphs, it is directly noticeable that the switching losses are negligible compared to the conduction losses. In this operating mode, the output current is approximately $I_L = 22$ A, while the amplitude of the ripple of the current is 27 A. Due to such a high ripple when the lower transistor is switched off, the current is negative and it is $I_{L\_min} = -5$ A. Then this switching off takes place according to the scenario described in 2.2.1.

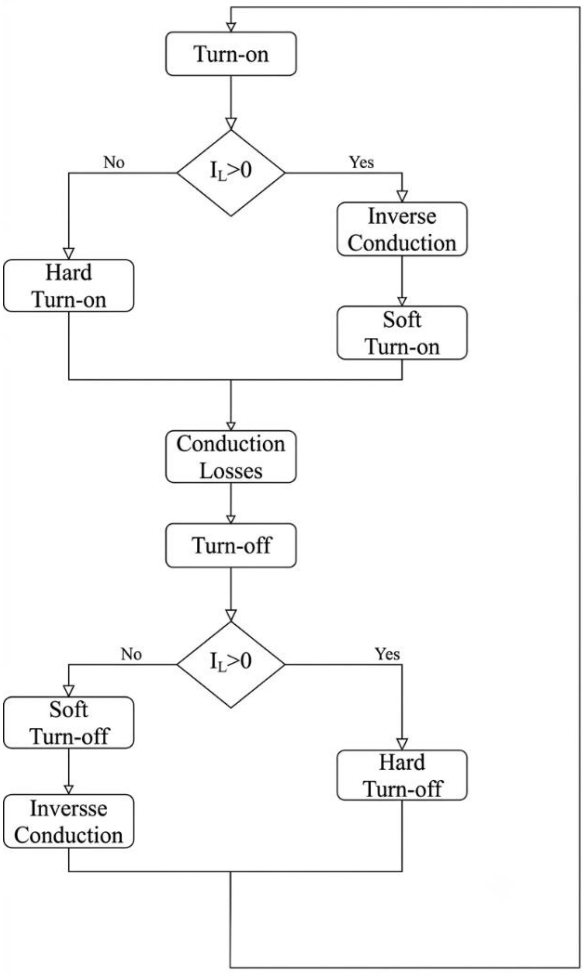


Figure 13. States that a transistor in a half-bridge passes through during a single switching cycle

Table I Parameters of the designed buck converter

Parameter	Value	Unit
Input voltage	10–72	V
Output voltage	5–70	V
Nominal power	1	kW
Switching frequency	125	kHz
Dead time	25	ns
Inductor	1,5	µH
Transistor	GaN [10]	/
Driver	[11]	/

From Figure 3, it can be seen that the overlap between the current I_{ch} *(t)* and the voltage v_{ds} *(t) is* very small, and the losses defined by equation (8) are very small. After the lower transistor is switched off, there is a period of dead time and switching on of the upper transistor. Switching on the upper transistor takes place according to the scenario described in 2.3.1 and also generates minimal losses. It is important to note that when this type of commutation occurs, switching off of the upper and the switching on of the lower one, it is realized according to scenario 2.2.1, then 2.3.1 and it results in minimum switching losses. The

combination of switching 2.2.1 and 2.3.1 can be achieved twice during one period only if the current when the upper transistor is switched on is negative, that is, if the ripple of the current is greater than the mean current of the consumer I_L. The total losses at both transistors in the case where the current ripple is less than the mean current I_L are shown in Figure 15. The loss in this case is now 10% higher.

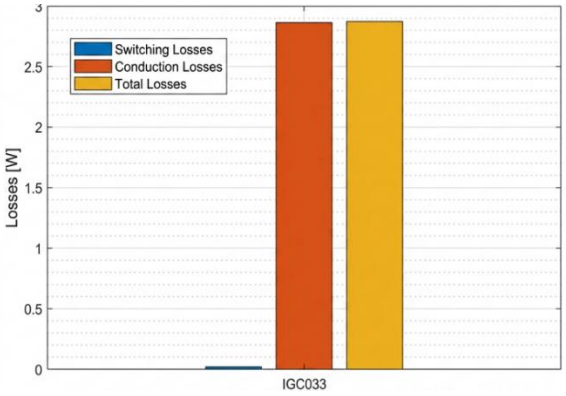


Figure 14. Total losses in both transistors in the half-bridge configuration

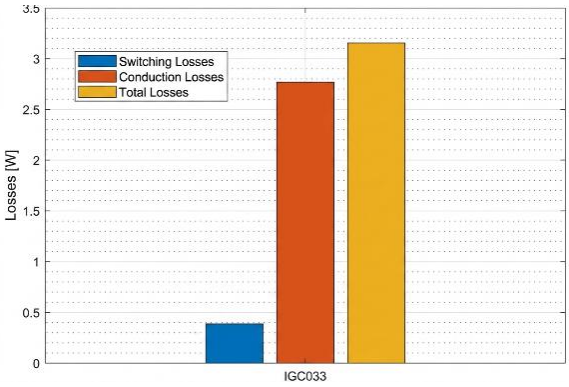


Figure 15. Total losses in both transistors in the half-bridge configuration at hard switching

4. EXPERIMENTAL RESULTS

In order to test and verify the analytical model, a 1 kW buck converter was designed (Figure 16). While designing and prototyping, special attention was paid to the arrangement of components on the printed circuit board to minimize the parasitic elements of the driver circuit and their impact on the switching process. Key data describing the converter prototype are given in Table I. Validation of the described commutation model was experimentally done on the setup given in Figure 17.

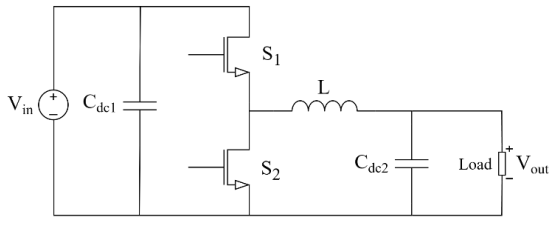


Figure 16. Topology of the designed power converter

The setup consists of:
(1) a laptop to communicate with the converter in real time;
(2) power supply;
(3) voltage and current probes with a bandwidth of up to 150 MHz;
(4) developed converter prototype;
(5) oscilloscope;
(6) passive resistance consumer $R_L = 2\ \Omega$.

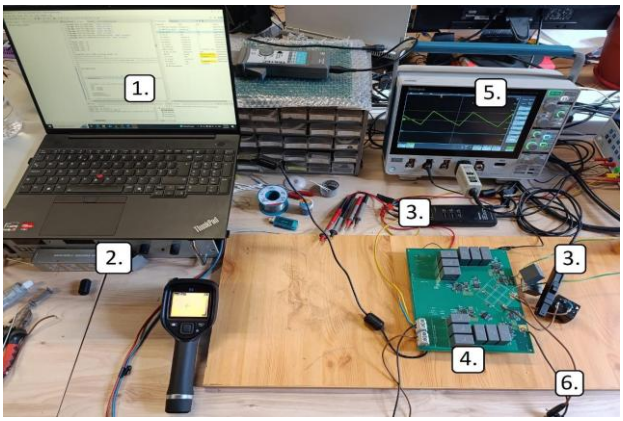


Figure 17. Experimental setup in the Laboratory for Digital Control of Converters and Drives, Faculty of Electrical Engineering, University of Belgrade

There are several methods to verify the switching model and the algorithm for estimating losses. One approach is to measure the total losses at the level of the entire converter, after which they are grouped into losses in copper conductors, reactive elements and auxiliary electronics. By subtracting these components from total dissipation, it is possible to indirectly estimate the losses at the transistors. However, in the converter designed, switching losses account for a relatively small proportion of the total losses, which makes this method subject to significant errors and deviations.

Therefore, the other approach was applied – direct assessment of the accuracy of the switching model by comparing the waveforms of voltage v_{ds} *(t)* and current I_{ch} *(t)*. As these two quantities are closely related, a good matching of voltage waveforms implies good matching of the current, and therefore an adequate estimation of switching losses.

A series of experiments were conducted in which the input voltage was changed in the range of $V_{in} \in [10, 60]\ V10$ V, while at the same time the duty cycle took values of $d \in$ [0,25; 0,5; 0,75]. The resistance of the passive load was fixed during all experiments and was 2 Ω.

The key parameter for verifying the developed model is the duration of the switching. The duration of the switching was tested on the setup shown in Figure 16 under different operating modes and further compared with the results of the analytical-numerical model. With an oscilloscope, the time it takes for the voltage v_{ds} *(t)* to change from 0 V to V_{dc}, when the lower switch is switched off (Figure 18), is measured.

Duration of switching for the lower and upper transistors for six different input voltages were measured. The experimental results were compared with the durations of switching obtained from the models over the entire

operating range of the voltage converter. The results are shown in Figure 19.

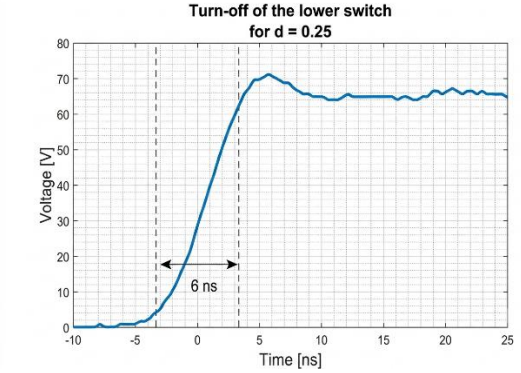
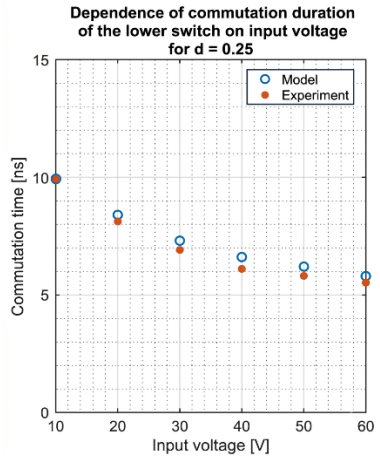
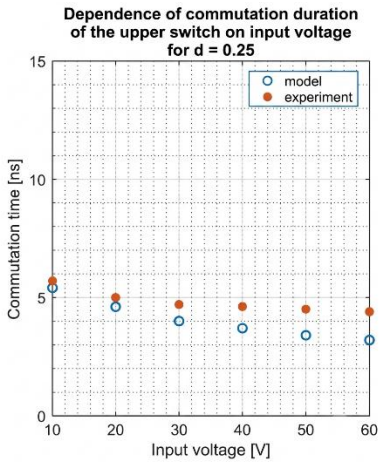


Figure 18. Changing the voltage of the v_{ds} when the lower transistor is switched off

From Figure 19, it can be concluded that the developed model follows the experimental values quite well, especially in the case of the lower transistor. At 10 V voltage, the model shows an almost perfect match with the measurements, with an accuracy of 99%.



a)



b)

Figure 19. The dependence of the switching duration on the input voltage: a) the lower transistor; b) the upper transistor in the half-bridge

However, as the input voltage increases, some deviation of the model is observed, with the largest difference observed at 40 V, where the accuracy drops to 92%.

On the other hand, the results for the upper transistor show a slightly poorer match with the experiment. The accuracy of the model decreases with increasing input voltage, reaching 75% at 60 V. This may indicate additional nonlinear effects or asymmetry in the influence of parasitic elements that are not fully covered by the actual model. Despite the discrepancies, the model demonstrates satisfactory accuracy, making it a useful tool for estimating switching times and estimating losses at transistors.

5. CONCLUSION

The paper describes in detail the processes of switching GaN transistors in the half-bridge configuration. A physical model of commutations is derived, which output parameters are the waveform of the current of the channel I_{ch} *(t)* and the waveform of the voltage drop on the channel v_{ds} *(t).* The parameters of interest are described in the function of operating modes. In order for the derived equations to be solvable without any introduction of approximations, with an appropriate software package, the relevant data were extracted from the datasheet of the specific transistor. The data extracted in this way were used to discretely solve the equations of the previously described physical model. For verifying the formed analytical-numerical model, a prototype of a buck converter based on GaN technology was developed and tested. The tests were done over the entire operating voltage range and the durations of the switching times resulting from the model and the experimental setup were compared. The model shows a very good match of over 92% with experimental tests of the switching duration of GaN transistors. The greatest deviations between the results obtained by the analytical-numerical model and the experimentally measured switching times on the prototype reach up to 25% for the upper transistor, which indicates the presence of certain effects that are not fully covered by the model and leaves room for further research.

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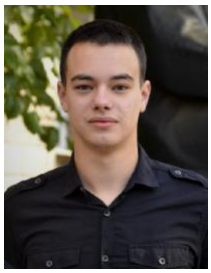
BIOGRAPHY



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Modelovanje gubitaka GaN prekidača na osnovu kataloških podataka

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Originalni naučno-istraživački rad

Ključne poruke

- Izvođenje algoritma za ocenu gubitaka GaN prekidača snage
- Poređenje tvrdih, mekih i polumekih prekidačkih procesa i izdvajanje strujnog doprinosa kanala i parazitnih kapacitivnosti
- Verifikacija modela kroz prototip sinhronog spuštača napona snage 1 kW

Kratak sadržaj

Prekidači zasnovani na savremenim poluprovodnicima velikog energetskog procepa, kao što je galijum-nitrid (GaN), sve češće se koriste u uređajima energetske elektronike. Zbog specifične strukture i sposobnosti da brzo menjaju radno stanje, standardni proračuni koji se koriste za određivanje gubitaka u silicijumskim prekidačima nisu primenljivi u ovom slučaju. Stoga je razvijen analitički model za procenu gubitaka kod GaN prekidača u konfiguraciji polumosta, koji se oslanja na podatke iz tehničke dokumentacije. Model uzima u obzir različite tipove komutacija, kao što su tvrdo, meko i polumeko komutovanje. Izvršeno je poređenje gubitaka pri mekom i tvrdom komutovanju prekidača u sklopu sinhronog spuštača napona. Na osnovu predloženog modela određena su vremena trajanja komutacija, koja su iskorišćena kako bi se verifikovao predloženi model na pretvaraču spuštaču napona snage 1 kW.

Ključne reči

GaN prekidači snage, model gubitaka, sinhroni spuštač napona

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